Keynote Address

Title: Space Transportation system Design- A System Engineering Approach

Speaker- Dr. M. V. Dhekane
Former Director, ISRO,
Thiruvananthapuram, India

Abstract:
Space Transportation system development is a complex multidisciplinary multiobjective task. This requires in depth understanding of almost all branches of science and engineering. Primary objective is to deploy a satellite in a specified orbit with utmost precision, with minimum fuel and thereby minimizing the cost per kg of the payload. Aerodynamics, propulsion technology,, structural engineering, Avionics, Computer science, Material science, manufacturing processes, Integration and testing and reliabilty engineering are some of important areas.

Avionics has the most important role to play. It Includes on board computer design, Electronics Hardware and software system design,communication engineering for temetry and telecommand, power system design, Navigation-Guidance and control Design, Actuator and sensors development and system validation.

It requires System engineering approach to design and develop a zero defect fault tolerent system considering the complex interactions of the subsystems.

ISRO has developed multiple launch vehicles-PSLV, GSLV and GSLV MKIII to cater to the needs of placing the satellites in the near Earth as well as Planetory missions. Reusable Launch Vehicle Development and Human in Space Mission are the new challenging endeavors of ISRO. Systematic project planning, following excellent Design Prctices,in depth analysis,extensive testing, periodic critical reviews, constant update of knowledge through structured Training programs and dedicated manpower is the key to Success.

Plenary Session 1:

Title: Space Technology in Navigation

Speaker: Hemachandran S.

Deputy Director, Inertial Systems
Production Entity at
ISRO Inertial System Unit (IISU),
Thiruvananthapuram, India

Abstract:

Navigation: Indian Regional Navigation Satellite System (IRNSS) is an autonomous regional satellite navigation system developed by ISRO (Indian Space Research Organization). It is renamed as NavIC (Navigation with Indian Constellation) by Honorable Prime Minister of India during dedicating to the nation. It has all the functionality of GPS signals except the fact that it is confined to Indian region. The Government of India approved the project in May 2006, with the intention of completing and implementing the system by 2016. The objective of the project is to establish an independent and indigenous regional space-borne navigation system for national applications. The NavIC design requirements call for a position accuracy better than 20m (2sigma) throughout India and a region extending around 1500 km. The system is expected to provide accurate real-time position, velocity and time observables for users on a variety of platforms with 24x7 service availability under all weather conditions. The NavIC system consists of a constellation of seven satellites and a supporting ground segment. Three of the satellites in the constellation will be placed in a near geostationary orbit and the remaining four in a geosynchronous inclined orbit of 29º inclination. Such an arrangement would mean all seven satellites would have continuous radio visibility with Indian control stations.

NavIC uses 24MHz bandwidth of spectrum in the L5-band (1164 – 1189 MHz) centered at 1176.45MHz and 16.5 MHz spectrum in S-band (2483.5 – 2500 MHz) centered at 2492.028MHz.

The satellites are kept in the following orbital slots

- 3 satellites in GEO (Geostationary Orbit) at 32.5°, 83° and 131.5° East
- 4 satellites in geosynchronous orbit placed at inclination of 29° with longitude crossing at 55° and 111.75° East. (Two spare satellites are also planned)

The NavIC constellation architecture consists of the following three segments like in any GNSS system:

Space segment: The NavIC satellites carry a navigation payload in a redundant configuration. A separate C-band transponder for precise CDMA ranging is included in the payload configuration. The important functions of the NavIC payload are: Transmission of the navigational timing information in the L5 band and S-band; Generation of navigation data on-board, CDMA ranging transponder for precise ranging. The navigation payload will have the following subsystems: NSGU (Navigation Signal Generation Unit), Atomic clock unit : comprising of Rubidium atomic clocks, clock management and control unit, frequency generation unit, modulation unit, high power amplifier unit, power combining unit and navigation antenna.

The NavIC spacecraft are dedicated for navigation services and they are configured to be of a class that can be launched by the PSLV launcher. The first satellite was launched in the summer of 2013. The full constellation was completed in April 28th, 2016.

Ground segment: The ground segment is responsible for the maintenance and operation of the NavIC constellation. It consists of : Master Control Center for spacecraft control and navigation, NavIC tracking and integrity monitoring stations, CDMA ranging stations, Uplinking and telemetry stations, Dedicated communication links between monitoring stations and master control center and timing enter with atomic clocks.

User segment: Specially designed receivers and antennas are needed to receive the NavIC signals. The receivers are also planned for receiving multi-constellation signals inclusive of GPS, GLONASS, Galileo and NavIC. It is planned to broadcast the time difference between the NavIC time and the time of the other constellations to enable the users to take advantage of the signals available to them.

NavIC has two services namely Standard Positioning Service (SPS) and Restricted Positioning Service (RS). SPS used BPSK modulated signal while RS signal used BOC(5,2) modulated (Binary Offset Carrier) signal. Both the signals are available in L5 and S band. RS signal is more robust, secured and precise compared to SPS signal. Unlike GPS or GLONASS system which are controlled by military agencies, NavIC is controlled by ISRO and ensure the free access of NavIC signals all the time. Specific text messaging scheme is unique in NavIC architecture.

GAGAN stands for GPS aided GEO augmented navigation, meaning the GPS navigation accuracy, integrity and availability are enhanced using a GEO satellite. The GPS timing signals are erroneous due to signal propagation through the troposphere, ionosphere and due clock related information. The GPS signal quality is not guaranteed all the time. The augmentation system like GAGAN observes the quality and other errors of GPS signal around Indian region using a set of ground monitoring station and uploads the information to GAGAN monitoring center. The monitoring center churn out the correction information and upload to GEO satellite viz GAGAN. Presently GSAT8, GSAT10, and GSAT15 are GAGAN

enabled GEO satellites. The correction information is sent out in L1 band with unique PRN code. Thus the signal can be received by any GAGAN enabled GPS receiver and correct the GPS signal timing more accurately. Typically one can receive GPS signal with less than 3 to 4 m accuracy.

Application: Global Navigation Satellite System (GPS, GLONASS, GALIEO, COMPASS) applications are many in different areas of activity. GNSS receiver becomes a de-facto feature of mobile phone and thereby enables many location based services. Many of those applications can be ported with navIC enabled receivers and Bhuvan web site link to reap the benefit in Indian region. Land survey, intelligent transportation, defence, civil aviation, shipping, precision agriculture, distributed precision timing, fisheries, survey, science, electric network, geographic Information system are some of the applications. Since NavIC signal is available in 24x7 from the same satellite, RF signal property can be studied extensively studied to model ionosphere and troposphere. Many scientific activities are being time-marked using GNSS time to understand the physical phenomenon. Adventure sports and Augmented Reality are new avenues of GNSS application.

Plenary Session 2:

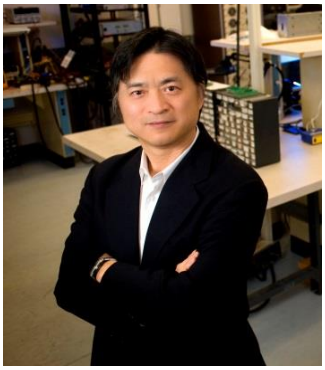
Title: Resource-constrained VLSI Systems Design for Signal Processing

Speaker: Dr. Amit Acharyya

PhD (University of Southampton, UK)
Associate Professor, Department of Electrical Engineering, Indian Institute of Technology (IIT), Hyderabad, India.

Abstract:
The focus of this talk is in resource-constrained VLSI systems design using signal processing algorithm-architecture holistic approach and the targeted application is healthcare technology. Several digital arithmetic techniques would be discussed that would enable the advancement in the state-of-the-art technologies. This will also be put in the context of the design and development of next-generation pervasive health-monitoring systems for the remote healthcare especially to tackle cardio-vascular diseases.

Plenary Session 3:



Title: Future Energy Electronics Center (FEEC) Introduction and Google Little Box Challenge Experience

Speaker: Jih-Sheng (Jason) Lai,
Ph.D. James S. Tucker Chair Professor,
Virginia Polytechnic Institute and State University, USA

Abstract:

With fast development of wide bandgap (WBG) semiconductor devices and their promise on superior conducting and switching features that allow ultrahigh-efficiency power electronics design. In July 2014, Google announced to hold a Little Box Challenge – a one-million US dollar inverter design competition. The initial entry exceeded more than 2000 teams, but only about 100 final report submissions, and only 18 teams were selected for the hardware testing, which was conducted at the US National Renewable Energy Laboratory (NREL). In the end only three teams passed the overall testing, and the winner was the one with highest power density. Virginia Tech is the only university team that went through all the tests successfully and was placed top three finalist. Major challenges of the design include how to deal with the low-frequency second harmonic ripples, output filter size minimization, electromagnetic interference (EMI), and thermal management. This presentation will discuss briefly on the figure of merit of WBG devices silicon carbide (SiC) and gallium nitride (GaN) and their selections. A summary review goes to how the teams select inverter circuit topologies, pulse width modulation techniques, double line frequency suppression, design of harmonic and EMI filters, and packaging techniques.

Plenary Session 4:

Title: Wearable devices for the healthcare

Speakers: Dr. Maryam Shojaei Baghini

Professor, Department of Electrical Engg.
IIT-Bombay, Powai, Mumbai, 400076, India

Abstract:

Recent trends in healthcare technologies are shifting the monitoring, medical tests and the preliminary diagnosis from clinics and hospitals to homes by medical devices which are readily usable by the individuals. This trend has also created many opportunities for leveraging the existing platforms for making more affordable medical devices. In this talk, a brief review and examples of the wearable devices with various aspects of their operation are presented. The talk will also include examples of the research and prototyping in our group in Electrical Engineering Department covering instrumentation, signal/data processing and communication.

Plenary Session 5:

Title: IOT and Machine Learning

Speaker- Shri. Pranav Chauhan,
Project Manager, TCS , Nagpur.

Abstract:

Brief about latest technologies used in IoT solution development . About the processes follows in IoT during the complete development life cycle. Like Agile Process: From smart vehicle to smart home devices , IoT deliveries are made using Agile methodology . Devops is mandatorily used during IoT software development , in order that they can develop , test and deploy software faster and more reliably . Microservices architecture follows during large IoT application development, wherein applications are built as a collection of different smaller services rather than one whole app.

Plenary Session 6:

Title: Telemetry & IT OT Cyber security

Speaker- Shri Prasad Pendharkar,
Project Manager, TCS, Nagpur.

Abstract:

Brief information on IT-Information Technology & OT-Operation Technology. IT-OT holistic view. Need of IT-OTconvergance.Importance of the three major factors like Process, people & Technology in cyber security, Details of the impact of recent past malware/ransomware attack on the industry. Current trends on OT cybersecurity industry is focusing.IT-OT Cybersecurity Standards industry is referring for OT cybersecurity like NIST & ISA99. Importance of the OT infrastructure safety in view of the current trend of going with cloud technology with high dependability on internet.Industry should focus on the Five major towers while carrying out the assessment of cybersecurity for their industry. Measures industry are taking to be ready to safeguard its critical OT assets.

Plenary Session 7:

Title: MEMS and IOT

Speaker- Dr. Rajendra M. Patrikar,
Professor, Center for VLSI and
Nanotechnology, VNIT, Nagpur.

Abstract:

The systems built for supporting the Internet of Things (IoT) have become important electronic systems today. recently their numbers have increased exponentially because of their application in several fields. Advances in MEMS technology showing that IOT can leverage several core functions and benefits of MEMS. MEMS devices can effectively meet the requirements of many IoT applications. IoT sensors and gateways are often required to be wireless and battery powered. Due to low per unit cost, it's usually cheaper to replace the entire unit than to reinstall it with a new battery. Thus any reduction in power usage extends the life of the devices. Some MEMS face the same power requirements as their larger counterparts. Others take advantage of different forces in electromagnetism for power scavenging or fluid dynamics to reduce their power usage without sacrificing functionality. The small form factor, cost-effectiveness, and low power requirements of MEMS devices make them an ideal field for IoT hardware innovation. Users generally want IoT devices to be small and unobtrusive in most of the applications. MEMS are by definition unobtrusive. But beyond user needs, in some IoT applications, the device might need to be added to an existing machine. There are several examples for this. A car has limited room for more hardware. In other cases like wearables and biomedical applications, small size is a critical requirement that must be met. Due to their small nature, MEMS meet and exceed these requirements. When deploying an IoT solution, scale is usually a major concern. For instance, when putting sensors to monitor weather and moisture levels on a farm field, there will need to be many devices seeded in each acre. Or consider an asset tracking solution in which there may be an extremely large (and variable) number of assets that need to be tracked. In other applications, such as shipping, a device may just be one-time use. MEMS are made through a CMOS process, which makes it easy and cost effective to produce them in mass quantities. As more devices and applications are added to IoT, MEMS will become more viable solutions. It's exciting to see how both of these technologies will grow and influence each other. It is commonly known that CMOS-MEMS Technology is used for Sensing and Actuation and also for power scavenging popularly is ued in smart phones.

For system designers, performance vs. power dissipation; it's one of the most delicate trade-offs for those who are developing smart sensors for the emerging IoT-based application space. This tradeoff often discussed through signal to noise ratio and designers

have to struggle to maintain it to high level for most of the functions. Within the broad space of performance, noise is often an important attribute to evaluate, as it can constrain component selection for key functional blocks in a smart sensor, which in turn can increase the power burden. In addition, noise behaviors can drive filtering requirements, which can influence the sensor's responsiveness to rapid changes in conditions and extend the time it takes to develop a quality measurement. In applications that support continuous observation (sampling, processing, communication), system architects often have to work through an adversarial relationship between noise and power, as the lowest noise solutions are rarely the ones that also offer the lowest power (within a particular functional class of devices). In this talk it will also be discussed that MEMS technology comes to rescue in these situations for signal processing also because of its low power requirements.